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ESTIMATION AND PREDICTION OF THE CLOCK PHASE FLUCTUATIONS AND TIME-INTERVAL ERROR

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Abstract – This paper describes the new method of time-interval-error (TIE) estimation and prediction. This method is very useful for standard clocks characterization and can be applied in high precision measurement and telecommunication systems with high resolution of the time-base. TIE can be easily and fast calculated using only two parameters obtained during calibration process. Moreover, it is very simple method for clocks comparison and can be applied in time-interval measuring systems (TIMS) for calibration or TIE calculation. This method allows to calculate an accumulated jitter and TIE as a function of the clock cycles. The measurement system, specially accommodated for jitter measurements and their application for estimations or predictions of jitter parameters will be also presented and discussed.

Keywords: jitter, time-interval error, time-interval measurements.

1. INTRODUCTION

In many cases of the measurement, control and data transmission systems, duration of the single operation is of milliseconds order or even only microseconds, at the system resolution of several or hundreds picoseconds order. Characterization of the clock phase fluctuations can be suitable for optimal selection and verification of the oscillators for applications in systems with high precision time-base. Moreover, knowledge of clock phase fluctuations can enable for TIE or maximal TIE estimation or uncertainty of measurement calculation for many types of TIMS [1 - 3].

It is not difficult to find convenient examples where such parameters are very important. For example: measurement systems of laser distance meters, measurement systems of LIDAR (Light Detection and Ranging), which has been used extensively for atmospheric research and meteorology, measurement systems of ultrasonic flowmeters, sequential imaging and in many measurements systems of modern atomics physics, such as time-of-flight monitoring systems or life-time measurements systems for an excited atomic states [4, 5].

New method of the clock accumulated jitter measurement is based on repeated measurement of time-intervals, which consists of determined clock period number [4].

High-resolution of the time-interval measurement system was obtained by using tapped delay line (TDL) implemented in single FPGA (Field Programmable Gate Array) device. Precision of the time-interval measurement depends on resolution of the delay-line, which strongly depends on parameters of the applied FPGA device. Using the FPGA device XC2VP4 (Virtex 2 Pro) the resolution is equal to70 ps, however for the XC4VLX25 device (Virtex 4) the resolution could be increased up to 50 ps [5].

The measurement system, presented in this paper enables for TIE estimation in range from several nanoseconds up to several seconds with precision dependent on the number of measurements.

Accumulated jitter of the clock signal or data stream is a result of phase fluctuations caused by different kinds of noise or distortions [1 - 3]. Phase fluctuations can be random, described by Gaussian distribution or determined, caused usually by the structure of measurement system. According to the standard clock signal of the measurement systems, jitter accumulated during single measuring cycle, which consists of integer number of the clock periods (as it is shown in Fig.1.) has important meaning.

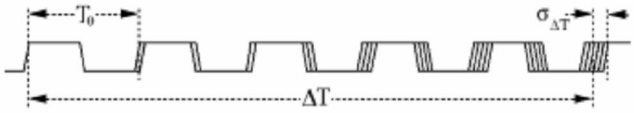

Fig.1. Accumulated jitter of the clock signal

In practice, most important parameter describing the accumulated jitter is standard deviation $\sigma_{\Delta T}$, calculated according to fluctuations of time-interval ΔT. It is possible to calculate an uncertainty of the time-interval determined by the N cycles of standard clock [5]. It should be pointed out, that sometimes the TIE caused by accumulated jitter can be many times greater than TIE caused by the interpolation of residual time-intervals between standard clock and oscillator, which is under test.

2. PRINCIPLE OF MEASUREMENT

Measurement of the clock accumulated jitter can be realized by the specially prepared high-resolution time-interval system [4]. Principle of such time-interval measurement is shown in Fig.2. The time-intervals between

events determined by the successive rising edge of the oscillator under test can be measured as the differences between time-stamps of such events related to the standard clock signal [4]. In this way the time-interval Δt_{mi} between first rising edge incoming after trigger and any successive rising edge of the oscillator can be given by the equation:

$$\Delta t_{mi} = \Delta t_{ki+1} - \Delta t_p + T_0 \cdot \left(N_{i+1} - N_0\right), \qquad (1)$$

where T_0 is the standard clock period, N_0 is the integer number of counts of the clock counter before trigger pulse, N_i is the integer number of counts of the clock counter before i-th clock under test rising edge, Δt_p is a time-interval between previous standard clock rising edge and the first rising edge after trigger pulse of the oscillator under test and Δt_{ki} is a time-interval between previous standard clock rising edge and the i-th rising edge of the oscillator under test.

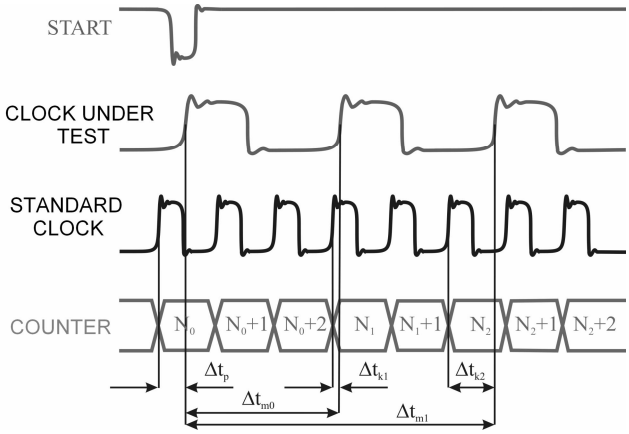

Fig.2. Principle of time-interval measurement

The time-intervals, measured as differences between time-stamps collected during many measuring cycles can be consider as random variables Δt_N, with Gaussian distribution of probability. Of course, standard deviation of the random variables Δt_N will be different than standard deviation of the tested oscillator period [5].

The standard deviation $\sigma_{\Delta tN}$ of Δt_N is generally given by

$$\sigma_{\Delta t_N} = \frac{\sqrt{N^a}}{c\sqrt{2\pi}}, \qquad (2)$$

where : $1 \le a \le 2$.

Parameter c depends from quality of oscillator and is given by

$$c = \frac{1}{\sqrt{2\pi}\sigma_\varepsilon}, \qquad (3)$$

where : σ_ε is a standard deviation of single oscillator period.

The standard deviation of the time-interval measured by standard oscillator depends significantly on the number N of oscillator cycles as it is shown in Fig.3. As it is shown above (2) only two parameters *a* and *c* are necessary for accumulated jitter characterization [5]. These parameters can be easily calculated from Gaussian distributions of earlier collected time-stamps. Knowledge of accumulated jitter characteristic (2), allows to predict a standard deviation for any time-interval.

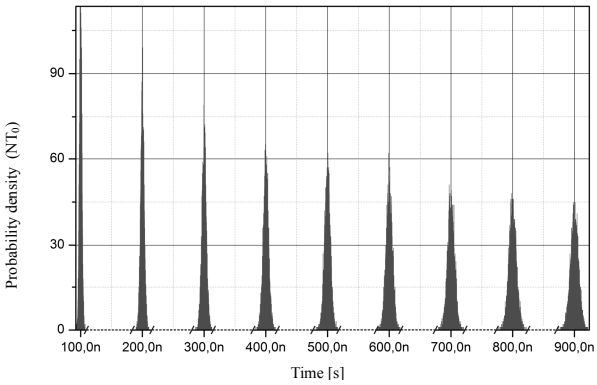

Fig.3. Modification of probability density function vs. time-interval measurement

TIE equal to the standard deviation $\sigma_{\Delta t}$ can be calculated from (1), and is given by

$$\sigma_{\Delta t} = \sqrt{\sigma^2_{\Delta t_N} + \sigma^2_q} \ . \qquad (4)$$

Quantization error σ_q can be calculated from INL (Integral Nonlinearity) characteristic of the measurement instrument. TIE caused by the system oscillator $\sigma_{\Delta tN}$ can be estimated during calibration process [5].

3. MEASUREMENT SYSTEM

Measurement of the accumulated jitter caused by phase fluctuations of oscillator based on multiple measurement of time-intervals, which consists of integer number of periods.

Measurements are realized in relation to the standard clock. From that reason the system contains two inputs: CLK_SYS and CLK_MEASURE. The block diagram of the measurement system is shown in Fig.4.

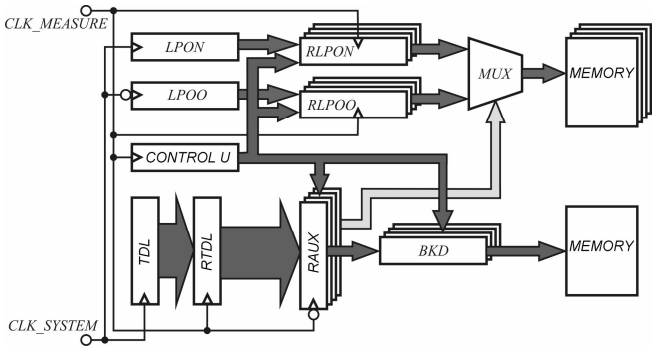

Fig.4. Block diagram of the measurement system

Time-stamps are registered and collected during each measuring cycle. Average delay-time of the single delay element is equal to 49,1 ps and number of the delay elements is equal to 102. Total delay time of the tapped-delay-line is greater than half of the standard clock period. Frequency of the standard clock is equal to 100 MHz. The number of clock cycles is registered by two consecutively working counters LPOO and LPON. One of these counters is incremented by the rising edge while the second one by

the falling edge of the standard clock signal. In this way the data can be asynchronously read-out from one of the counter. It should be pointed out, that the rising edge occurs at the inputs CLK_SYSTEM and CLK_MEASURE asynchronously. The setup time of the counter implemented in programmable device Virtex XC4VLX25 is about 2 ns. Information about standard clock phase, which is registered in the tapped-delay-line register RTDL and auxiliary registers of tapped-delay-line RAUX is also used for the clock counters selection.

Each time-stamp consists of two parts. The most significant of them is taken from one of the auxiliary registers of clock counters RLPON or RLPOO. The least significant part is taken from one of the auxiliary registers of tapped-delay-line RAUX. Every time, 102 bit data from RAUX register is converted by two-stage code converter BKD. The first stage converts data from thermometric code to 1 of N, while the second converts the data to the natural binary code. In such way 102 bit data word is compressed to only 8 bits. Physically both parts of time-stamp are separated and stored in different part of RAM memory. The total length of time-stamp is equal to 40 bits (32 + 8). Process of data conversion costs a lot of time. From that reason the data converter consists of parallel working sections. Moreover, many of functional blocks of the measurement system were multiplied to increase the speed of data transfer. Parallel signal processing of the input data shown in Fig.4 enables fast data collection. Intensity of the rising edges, occurring at the input CLK_MEASURE can achieve the value of 10^8 s^{-1}.

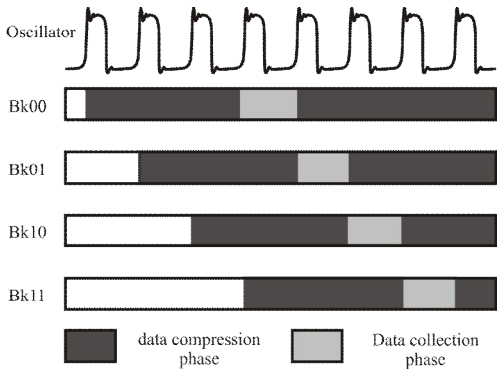

Fig. 5. parallel signal processing

First rising edge which occurs at the input CLK_MEASURE after trigger, writes states of the tapped-delay-line register and states of the clock cycles counters into the auxiliary registers of number 00.

Data written into the auxiliary register is converted by appropriate section of the data converter BKD. Each next rising edge writes data to the successive auxiliary register. When data is writing to the auxiliary register 11, the data from the auxiliary register 00 is collected in memory block as it is explained in Fig.5. Data conversion time is strongly limited (to 4 ns) because four sections of the BKD converter are working simultaneously at the same time. FPGA devices contain many CLB (Configurable Logic Blocks) in their structure. Each CLB of Virtex FPGA device consists of two slices. Each slice contains two Flip-flops, two four-inputs LUTs (Look-Up Table), multiplexers and XOR logical gates [4].

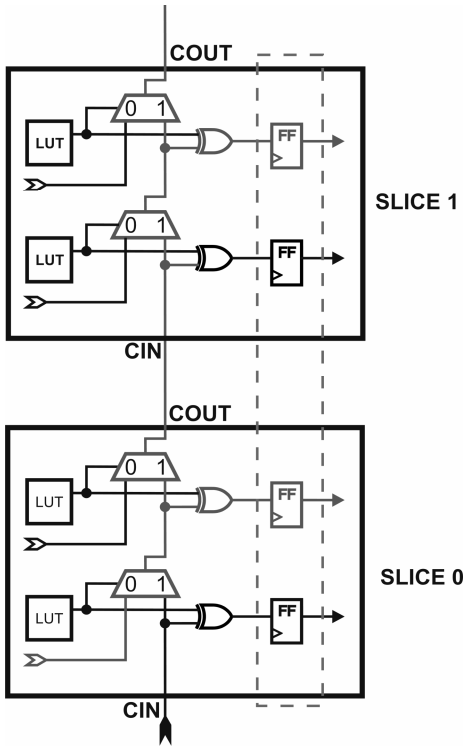

Fig.6. Tapped-delay-line implementation

The TDL is implemented inside single column of CLB, using very fast connections between COUT and CIN, as it is shown in Fig.6. Such construction of delay-line enables very high resolution of the oscillator phase measurement. The resolution depends on FPGA device architecture and is equal to 70 ps for XC2VP4 (Virtex2 Pro) or 50 ps for XC4VLX25 (Virtex4) device.

Delay of the single TDL element strongly depends on the propagation time of the signal through three multiplexers which are inside single CLB of the FPGA device. Appropriately configured LUTs enable to fed the reference signal to the input of one of the D flip-flop. Those flip-flops form the elements of the tapped-delay-line register RTDL. It should be pointed out that structures of the TDL were described in VHDL language using the standard library UNISIM.V.Components. the place of the TDL implementation inside the structure of the FPGA device is determined by the User Constrains File [4].

4. SIMULATIONS AND MEASUREMENT RESULTS

The measurement module has relatively high but limited resolution (50 ps). From that reason, standard deviation of the measured time-interval $\sigma_{\Delta T}$, will be increased of quantization error σ_q. For resolution q = 50 ps the quantization error σ_q is about 20,5 ps [5].

In case when short-time stability of both oscillators is very high and frequencies are almost equal, quantization process causes an additional fluctuations, shown in Fig.7.

Such fluctuations are caused by determined shift of the beginning of (i+1)-th time-interval, which is simultaneously end of the i-th time-interval inside single bin of quantization. Assuming that time-interval between the rising edge of both oscillators will be given by

$$\tau(t,T_0)=\frac{t}{T_0}|T_0-T|, \tag{5}$$

where: T is a period of tested oscillator, and T_0 is a period of standard oscillator.

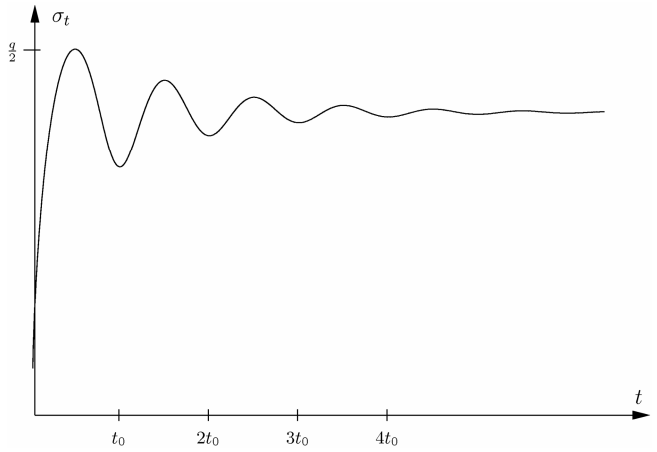

Fig.7. Quantization error influence on time-interval measurement

The time-interval t_0, needed to shift the rising edge of tested oscillator across single quantization bin q can be calculated from the equation

$$q=\frac{T_0}{N_{TDL}}=\frac{t_0}{T}|T_0-T|, \tag{6}$$

where – N_{TDL} is the number of TDL elements.

Period of fluctuations caused by quantization process is equal to the time-interval t_0 given by

$$t_0=\frac{TT_0}{N_{TDL}|T_0-T|}. \tag{7}$$

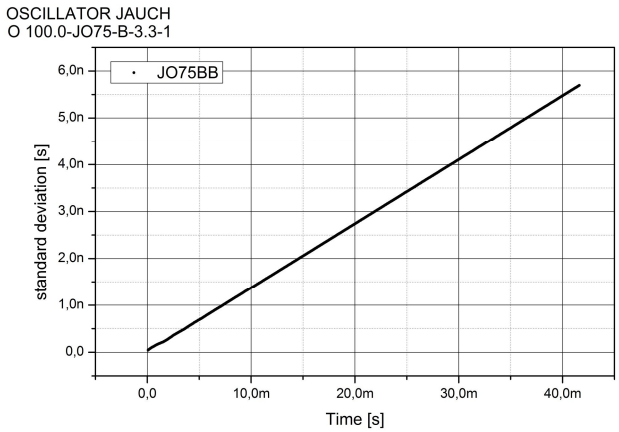

Fig.8. Characteristic of the standard oscillator

Usually, as it was pointed out earlier, for high-resolution TIMS, TIE caused by phase fluctuations of standard oscillator is greater than the error caused by quantization during interpolation. From that reason the error $\sigma_{\Delta tN}$ of different types of oscillators has been measured,

Algorithm of the $\sigma_{\Delta tN}$ measurement consists of two steps. First step is the calibration process which enables for standard clock characterization and calculation of the parameters *a* and *c*. In that case signals from two oscillators of the same type or from three different oscillators (coupled respectively in pairs) are fed to both inputs CLK_SYSTEM and CLK_MEASURE [5].

Knowledge of the characteristic parameters of the standard clock allows to find the characteristic parameters for any other oscillator. According to the first step two oscillators Jauch O 100.0-JO75-C-3.3-1 were tested. The result of calibration is shown in Fig. 8. The measured parameters for that oscillators are respectively c = (1,007 ± 0,011)·10^{-6} s and a = 1,9564 ± 0,0014.

Knowing parameters *a* and *c* obtained in the calibration process, it is possible to measure standard deviation of any other oscillator. In this case, reference oscillator 100.0-JO75-C-3.3-1 and oscillator under test O 100.0-JO75-B-3.3 -1 were used. The result of measurement is shown below, in Fig.9.

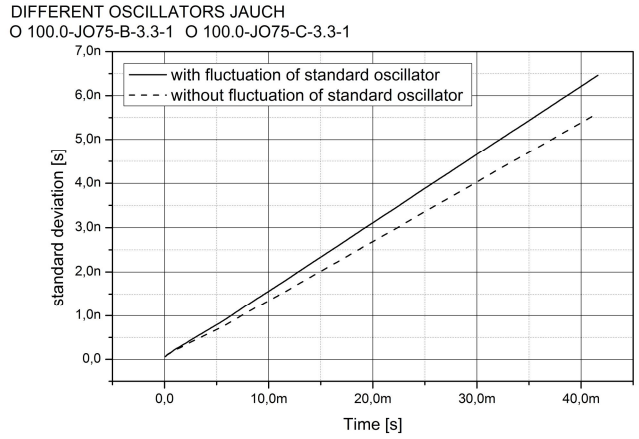

Fig.9. Characteristic of the oscillator under test

Taking into account the results of calibration, the pair of characteristic parameters for tested oscillator were received:

c = (1,386 ± 0,016)·10-6 s and a = 1,9960 ± 0,0016.

Next, during successive verification step both oscillators were exchanged. It means, that now as standard oscillator was applied the oscillator, which was earlier used as oscillator under test. The result of test is presented in Fig. 10. The measured parameters for that oscillators were respectively:

c = (1,403 ± 0,006)·10−6 s and a = 1,9966 ± 0,0006.

Similar results obtained for the calibration process using the oscillator O 100.0-JO75-B-3.3-1 and the results obtained during measurement process for two different oscillators confirm theoretical model.

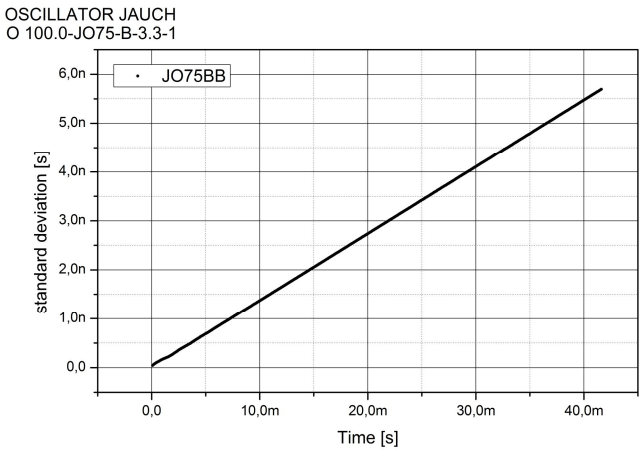

Fig.10. Characteristic of the standard deviation for oscillator O 100.0-JO75-B-3.3-1

In this way, the proposed method is useful to estimate of the TIE caused by clock phase fluctuation.

The method can be applied also above the range of 40 *ms* where coefficients *a* and *c* could be estimated. A result of such measurement is shown in Fig.11, below.

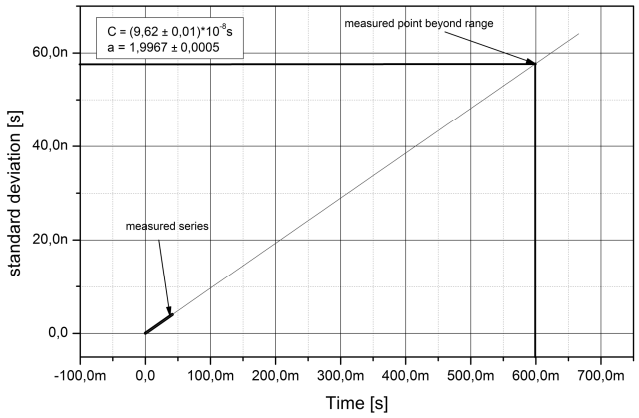

Fig.11. Prediction of the clock phase fluctuation

In this case estimated standard deviation have a value $\sigma(t) = (57{,}673 \pm 0{,}023)\cdot 10^{-9}$ s, when measured standard deviation $\sigma_m(t) = (57{,}6720 \pm 0{,}0003)\cdot 10^{-9}$ s.

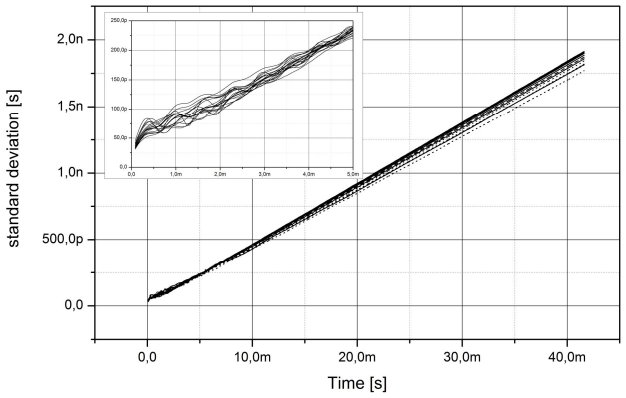

Fig.12. Characteristics of quartz oscillators CFPS-73

Both measured and estimated values are similar. It means, that measurement and prediction gives comparable results. This method enables prediction of TIE caused by clock phase fluctuation.

For oscillators of the same type distribution of standard deviation can be also measured as shown in Fig.12. For example, group of twenty quartz oscillators produced by Rakon Limited were tested.

Visible fluctuations of standard deviation are changing from *0,0007 s* to *0,0025 s*. Those values are equivalents of differences between oscillators periods in range from *0,2 fs* to *0,7 fs*.

Such small differences between periods give following differences between parameters c and a:

- $c_1 = (4{,}457 \pm 0{,}014)\cdot 10^{-8}$ s, $a_1 = 1{,}9811 \pm 0{,}0018$;
- $c_2 = (4{,}13 \pm 0{,}02)\cdot 10^{-8}$ s, $a_2 = 1{,}983 \pm 0{,}003$.

Knowing parameters *a* and *c*, it is possible to estimate the standard deviation and TIE for any time-interval. For example, standard deviations for time interval equal to t = 1s are:

- $\sigma_1(t=1\text{ s}) = (4{,}457 \pm 0{,}014)\cdot 10^{-8}$ s,
- $\sigma_2(t=1\text{ s}) = (4{,}13 \pm 0{,}02)\cdot 10^{-8}$ s.

For comparison other quartz oscillators produced by Gyer electronic KXO-V96 have been measured. Results of measurements are shown in Fig. 13.

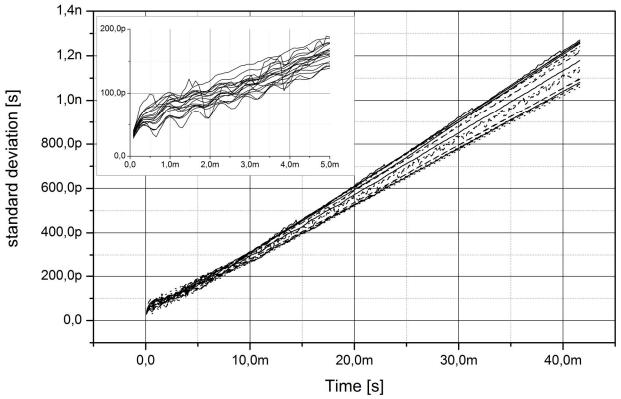

Fig.13. Characteristics of quartz oscillators KXO-V96

Also, in this case fluctuation of standard deviation characteristics were observed. Differences between oscillators periods were changing from *0,05 fs* to *0,8 fs*. Differences between parameters c and a are following:

- $c_1 = (2{,}822 \pm 0{,}024)\cdot 10^{-8}$ s, $a_1 = 1{,}9534 \pm 0{,}0005$;
- $c_2 = (2{,}296 \pm 0{,}012)\cdot 10^{-8}$ s, $a_2 = 1{,}9356 \pm 0{,}0028$.

For time interval equal to t = 1*s*, the appropriate standard deviation are following:

- $\sigma_1(t=1\text{ s}) = (2{,}822 \pm 0{,}024)\cdot 10^{-8}$ s,
- $\sigma_2(t=1\text{ s}) = (2{,}296 \pm 0{,}012)\cdot 10^{-8}$ s.

In such way, the best oscillator from group of quartz oscillators could be chosen and used as reference oscillator.

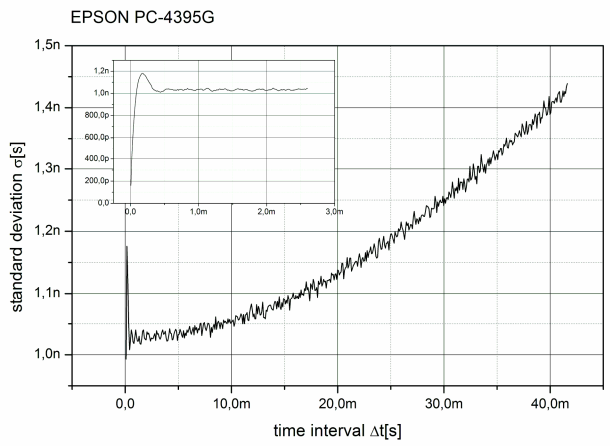

Fig.14. Characteristic of the PLL oscillator

Discussed method can be also applied to other types of oscillators. Phase-locked loop oscillators, oven quartz oscillators and many types of another oscillators can be tested exactly in the same way as simple quartz oscillators.

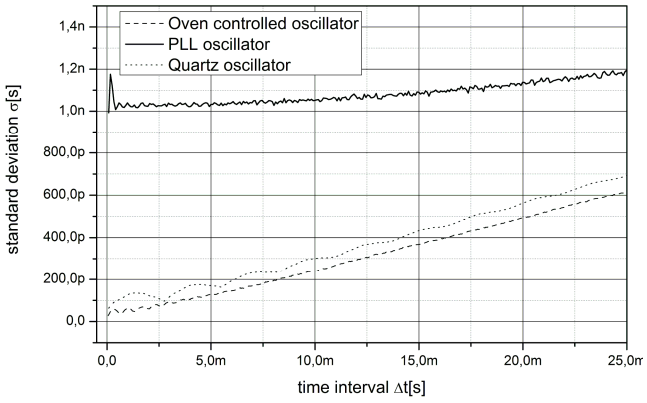

Fig.15. Comparison of different oscillator types in range up to 25ms

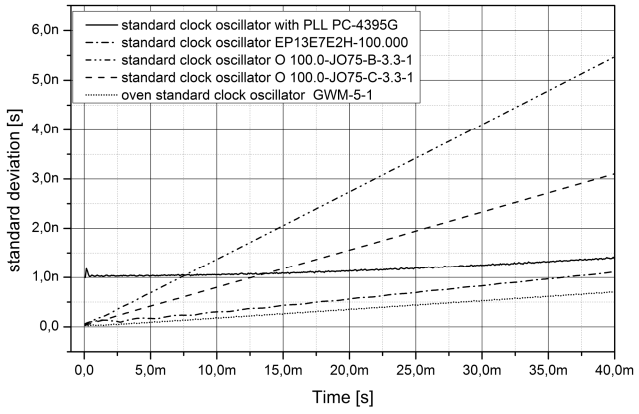

Fig.16. Comparison of different oscillator types in range up to 40ms

As a sample of PLL oscillator, which characteristic is shown in Fig.14, the Epson PC-4395G oscillator has been measured [6].

The results of comparison of different types of oscillators show, that presented high-resolution measurement system applied for oscillators tests allows to compare different types of oscillators as it is shown in Fig.15. and Fig.16. This method enables for optimization of the measurement system, limiting TIE in the range of measurement.

5. CONCLUSIONS

The results obtained during measurements and simulations allow to point out, that presented method enables for TIE estimation and prediction for different types of oscillators. Range of analysed time-intervals depends on size of RAM memory. Standard deviation of TIE estimator depends from the delay line resolution and the number of measurement cycles. Measurement of parameters *a* and *c* allows to verify oscillator for different types of data transmission and measurement applications..

ACKNOWLEDGMENTS

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